gate transistor having a first source/drain connected to a bit line and the second transfer gate transistor having a first source/drain connected to a complement bit line and each transfer gate transistor having a gate connected to a word line; and

first and second pull-down transistors configured as a storage latch, the first pull-down transistor having a first source/drain connected to a second source/drain of said first transfer gate transistor and the second pull-down transistor having a first source/drain connected to a second source/drain of said second transfer gate transistor, both first and second pull-down transistors having a second source/drain connected to a power supply voltage node;

wherein the first and second transfer gate transistors each **have a first width and** include a gate oxide layer having a first thickness, the first and second pull-down transistors each **have a second width and** include a gate oxide layer having a second thickness, and **a product of the first width and** the first thickness is **[different from]** **greater than or equal to a product of the second width and** the second thickness.

~~13~~. (amended) A semiconductor circuit comprising:

a first transistor having **a first width and** a first gate including a gate oxide layer having a first thickness; and

a second transistor having **a second width and** a second gate including a gate oxide layer having a second thickness, wherein **a product of the second width and** the second thickness is greater than **a product of the first width and** the first thickness.

REMARKS

Claims 1-5 and 13-19 are pending in the present application. Claims 1 and 13 were amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 103 (Obviousness)

Claims 1-5 and 13-19 were rejected under 35 U.S.C. § 103(a) as